Calculators not allowed.

1. (5 marks) In the lab you see the following program listing. Carefully examine this listing and answer the questions that follow. *Each question refers to a specific line in the listing*

.EQU STORAGE, 0x00001000

# ===== start of code =====

movia r6, Y #line 1

stw r6, 0(r6) #line 2

or r6, r0, r0 #line 3

# ===== more code here=====

.ORG STORAGE

W: .word 9, 8, 7

X: .half 6, 5

Y: .skip 4

1. The instruction at line 1 (movia) is an alias for what instruction(s)?

\_\_\_\_\_\_\_\_\_\_orhi then addi\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

1. What binary instruction is generated by the assembler for the instruction at line 3?

\_\_\_\_\_\_\_\_\_0b 00000 00000 00110 010110 00000 111010 / 0x000CB03A\_\_\_\_\_\_\_\_\_\_\_\_\_

1. What value is stored by the instruction at line 2 (assuming line 1 has already executed)?

\_\_\_\_\_0x00001010\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

1. What is the purpose of the instruction at line 3?

\_\_\_\_\_to clear register r6 (set r6 equal to 0x00000000)\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

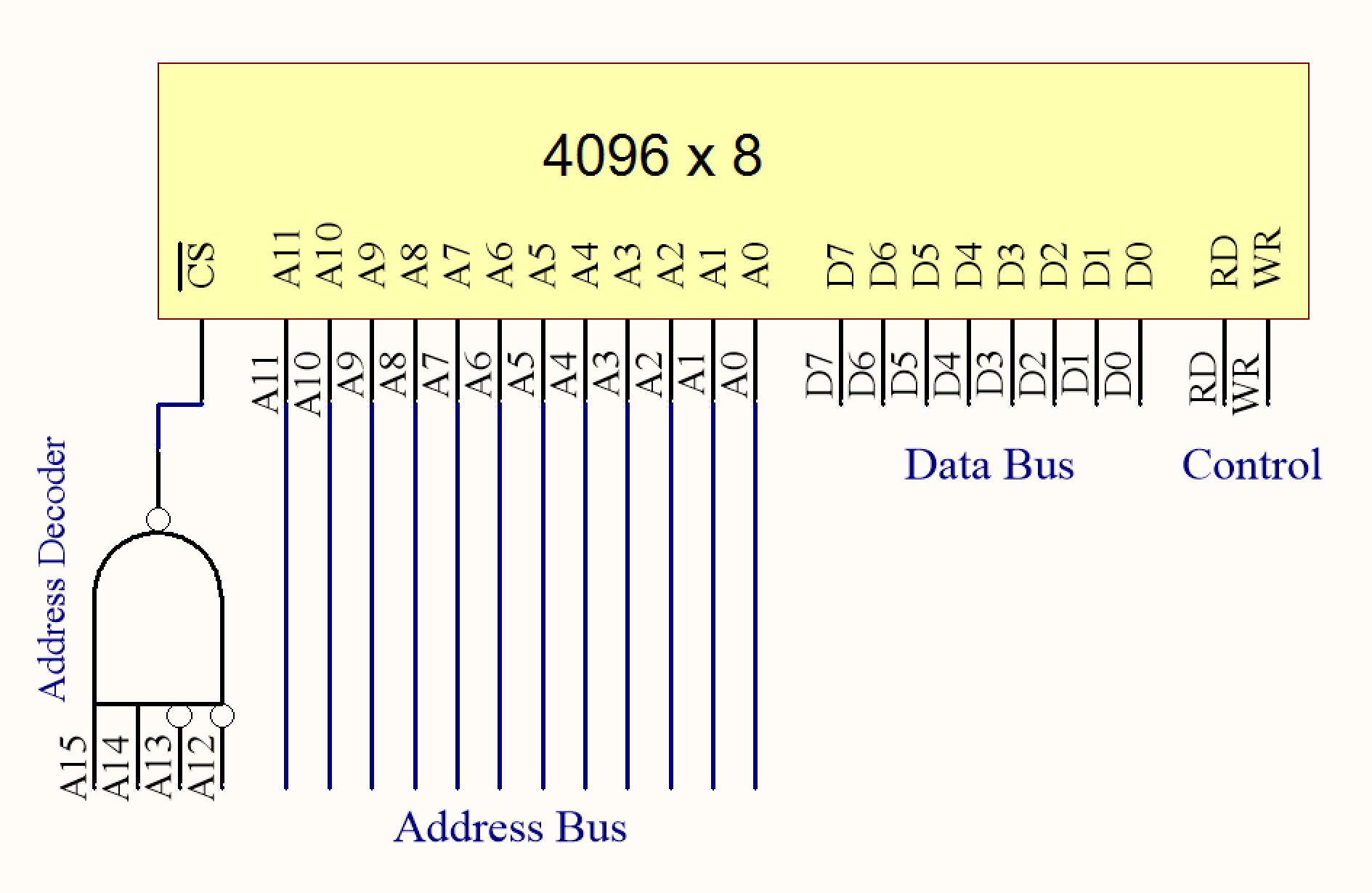
1. (2 marks) Explain why switch debouncing is necessary when interfacing real switches to digital circuits:

\_\_\_\_\_A real switch tends to produce a less-than-ideal voltage signal as it is pressed and\_\_\_\_\_\_\_

\_\_\_\_\_released. This results in multiple edges when a single edge is expected. \_\_\_\_\_\_\_\_\_\_\_\_\_\_

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1. (5 marks) Draw and label a block diagram of a single port **4096x8** read write memory chip. Ensure that the memory chip includes **an active low chip select line, all address lines, all data lines, a read line, and a write line**. The memory is to be interfaced to a system with a **16-bit address space** **(use a NAND gate to perform the address decoding)** and this block of memory is to span the address range **0xC000 to 0xCFFF**.



1. (3 marks) When a subroutine is called from the main program code using the **call** instruction, the processor branches to the area of memory where the subroutine is stored by updating the program counter with the address of the subroutine. Explain how the processor is redirected to continue to execute the instructions that follow the call instruction in the main program code following completion of the subroutine. Discuss the instruction(s) required and the registers involved:

\_The ret instruction is placed at the end of the subroutine. This instruction takes return \_\_\_\_\_\_

\_address (ra) (or r31) and places it back into the program counter.\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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